XLR-PINOUT
PIN1 = SHIELD
PIN2 = a, +
PIN3 = b, -

✳ = INPUT TRANSFORMER OPTIONAL

INPUT A
OUTPUT A
INPUT B
OUTPUT B
B1 B2 B3 B4
T1 T2 DCN308840
JR1 JR2 JR3 JR4 0
0dBu
H1A H1B H1C H1D 10k
C315 C316 C317 C318 33p
R300 R301 R316 R317 10
C300 C306 1µ0
C301 C307 1µ0
R302 R319 5k6
R303 R318 11k
R304 R320 620
R305 R321 510
C302 C308 10n
C303 C309 4n7
I300B I301B I300A I301A NE5532
R306 R322 10
HI/LO CUT
SL1-B SL1-A
R307 6k8
I101B NE5532
C319 C320 22µ/16V
FRNT_INA FRNT_INB
TO SHEET 2
R313 10k
R314 10k
I302A I302B NE5532
S2-A
MONO BRIDGED
LEVEL CONTROL A
LEVEL CONTROL B
Part of 87128A
VR1 VR2 10kB
CN4X-5 CN4X-6 CN4X-7 CN4X-3 CN4X-4 CN4X-1 CN4X-2
CN4-5 CN4-6 CN4-7 CN4-3 CN4-4 CN4-1 CN4-2
R310 R312 R326 R328 3R9 33
C304 C310 47p
R311 R327 22k
I201B NE5532
DUAL PARALLEL
S4-A S4-B S4-C S4-D
I600-P I300-P I301-P I302-P
C311 C312 C313 C314 0µ1
+15V -15V +UB -UB
GND LIFT
CN38 CN33
C305 4µ7
S3-B
TL072
NE5532
BC327 BC337 2N3906 2N3904
1N4148
MUTD
FROM SHEET 3
R620 470k
R621 22k
R622 100k
R623 2k4
Q620 Q621 BC337
-15.6V
D602 1N4148
87128A
CN7X-3 CN7X-10 CN7X-8 CN7X-5 CN7X-9 CN7X-7 CN7X-1 CN7X-6 CN7X-4 CN7X-2
CN7-3 CN7-10 CN7-8 CN7-5 CN7-9 CN7-7 CN7-1 CN7-6 CN7-4 CN7-2
LIMIT_B FROM SHEET 2
LIMIT_A FROM SHEET 2
PROTECT
D23 D21 D19 D20 D27 D26 D22 D24
RED GREEN
POWER ON
R630 R631 4k7
D29 D28
DISPLAY ADJUST B
DISPLAY ADJUST A
VR600 VR601 4k7
R601 R611 6k8
D234 D233 1N4148
Q600 Q610 2N3906
Q601 Q611 BC327
Q602 Q612 BC337
Q603 2N3904
R602 R612 5k6
R603 R613 2k4
R604 R614 5k6
R605 R615 220k
D600 D601 1N4148
R606 R616 4k7
C603 C613 10µ
R607 R617 30k
R608 R618 5k6
I600A I600B TL072
DISPLAY B
DISPLAY A
FROM SHEET 2
CN2B-1 SP_B_OUT
CN2A-1 SP_A_OUT
R600 R610 20k
C600 C610 10µ

TL072 NE5532
BC327 BC337
2N3906 2N3904
AC VOLTAGE 1000 HZ, MEASURED WITH VTVM
DC VOLTAGE MEASURED WITH VOLTMETER 100kOHM/V

ALTERATIONS RESERVED!

SYMB.	REVISION	DATE	NAME
I	153/99	6.12.99	Stangl
H	100/98	10.98	Lang
G	78/98	09.98	Lang
F	56/98	06.98	Lang
E	88/97	12.97	Lang
D	115/96	10.96	Lang
C	26/95	3.3.95	Brandl
B	156/94	8.12.94	Taffner
A	103/94	13.9.94	Brandl

Last modified: 06.12.1999 12:02:40
Last plotted: 17.10.2000 09:41:02

	DATE	NAME
DSG'D		Taffner
CHK'D	3.3.95	Brandl M.
APP'D		

DYNACORD

86208I MAIN_PCB

CIRCUIT DIAGRAM 1/3

348724 2-

L1600